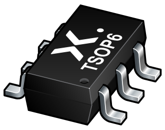


PBLS6002D-Q

60 V, 1 A PNP/NPN loadswitch double transistor

26 October 2023 — Product data sheet

1. General description

PNP low V_{CEsat} transistor and NPN Resistor-Equipped Transistor (RET) in a SOT457 (SC-74) small Surface Mounted Device (SMD) plastic package.

2. Features and benefits

- Low V_{CEsat} transistor and resistor-equipped transistor in one package
- Low threshold voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

4. Quick reference data

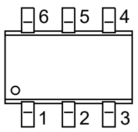
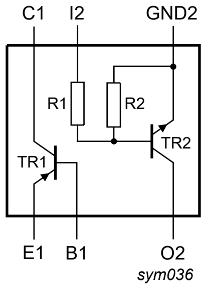
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	-60	V
I_C	collector current		[1]	-	-	-1	A
R_{CEsat}	collector-emitter saturation resistance	I_C = -1000 mA; I_B = -100 mA; T_{amb} = 25 °C	[2]	-	255	340	mΩ
TR2; NPN resistor-equipped transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	50	V
I_O	output current			-	-	100	mA
R1	bias resistor 1 (input)			3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	

[1] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.
[2] Pulse test: t_p ≤ 300 µs; δ ≤ 0.02

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 **TSOP6 (SOT457)**	
2	B1	base TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBLS6002D-Q	TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PBLS6002D-Q	F2

8. Limiting values

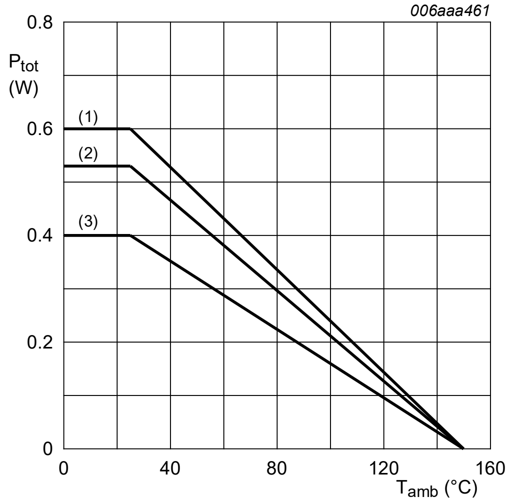
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1; PNP low V_{CEsat} transistor						
V_{CBO}	collector-base voltage	open emitter		-	-80	V
V_{CEO}	collector-emitter voltage	open base		-	-60	V
V_{EBO}	emitter-base voltage	open collector		-	-5	V
I_C	collector current		[1]	-	-700	mA
			[2]	-	-850	mA
			[3]	-	-1	A
I_{CM}	peak collector current	$t_p \leq$ 1 ms; single pulse		-	-2	A
I_B	base current			-	-300	mA
I_{BM}	peak base current	single pulse; $t_p \leq$ 1 ms		-	-1000	mA
P_{tot}	total power dissipation	$T_{amb} \leq$ 25 °C	[1]	-	250	mW
			[2]	-	350	mW
			[3]	-	400	mW

Symbol	Parameter	Conditions		Min	Max	Unit
TR2; NPN resistor-equipped transistor						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage			-10	30	V
I_O	output current			-	100	mA
I_{CM}	peak collector current			-	100	mA
P_{tot}	total power dissipation		[1]	-	200	mW
			[2]	-	200	mW
			[3]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	400	mW
			[2]	-	530	mW
			[3]	-	600	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.
[3] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.



(1) Ceramic PCB, Al_2O_3, standard footprint
(2) FR4 PCB, mounting pad for collector 1 cm^2
(3) FR4 PCB, standard footprint

Fig. 1. Power derating curves

9. Thermal characteristics

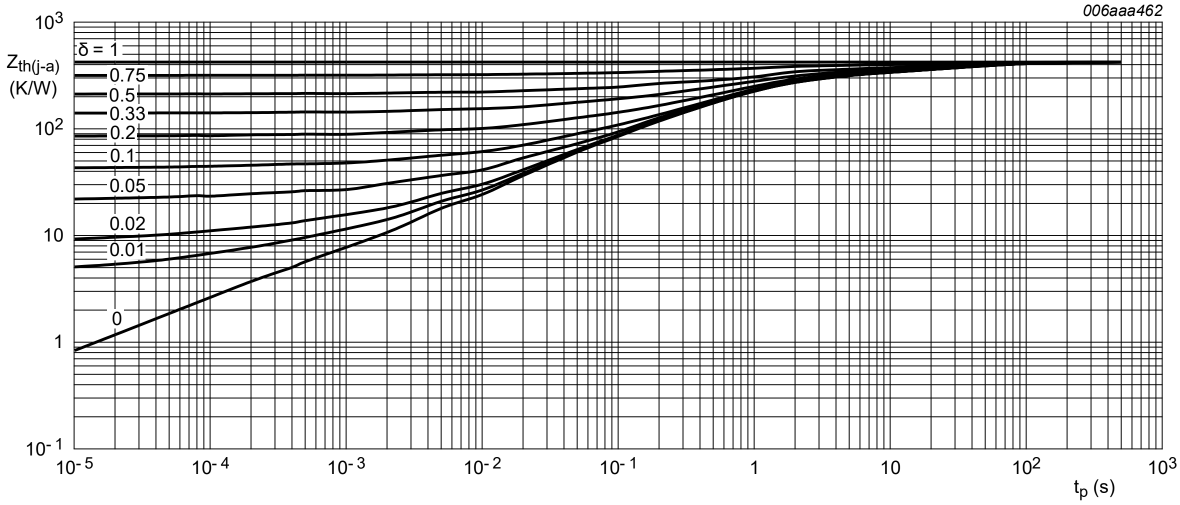
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	312	K/W
			[2]	-	-	236	K/W
			[3]	-	-	208	K/W
TR1; PNP low V_{CEsat} transistor							
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	105	K/W

[1] Device mounted on an FR4 PCB, single-sided, copper, tin-plated and standard footprint.

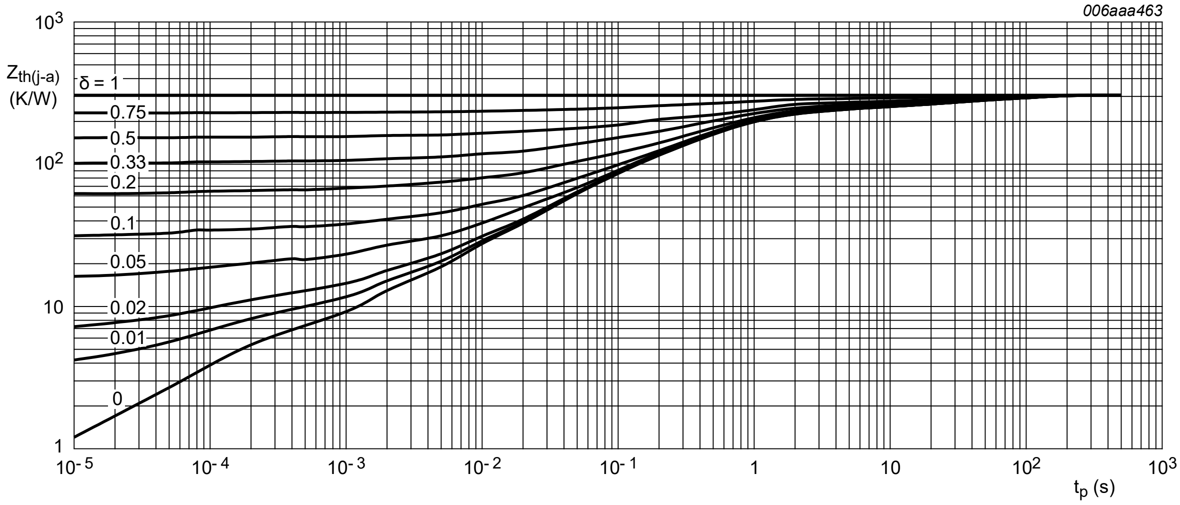
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.



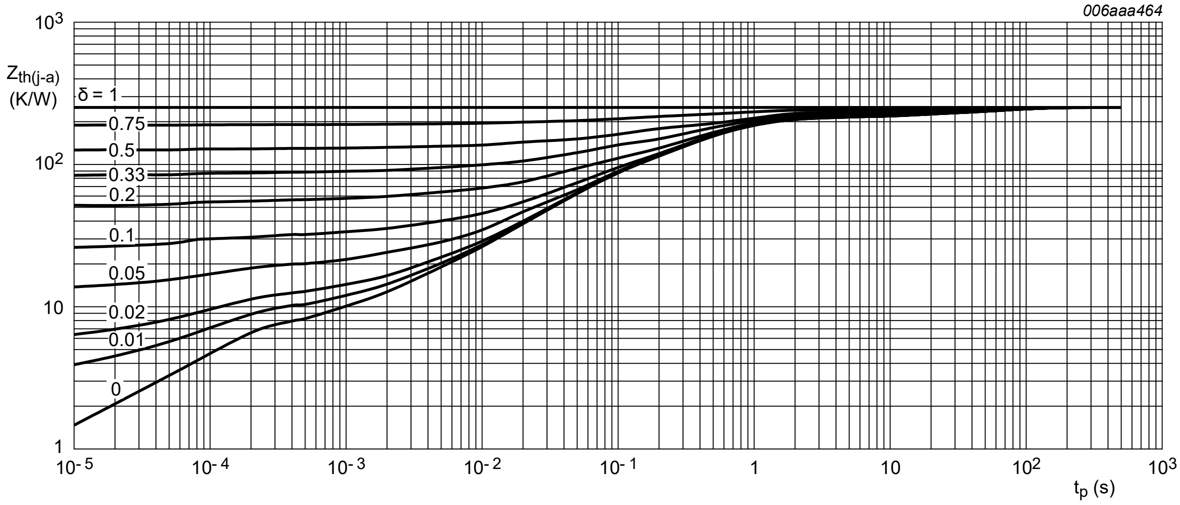
FR4 PCB, standard footprint

Fig. 2. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm^2

Fig. 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al_2O_3, standard footprint

Fig. 4. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

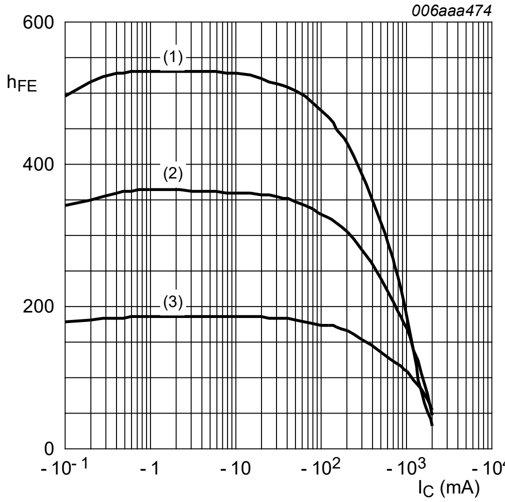
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor							
I_{CBO}	collector-base cut-off current	V_{CB} = -60 V; I_E = 0 A; T_{amb} = 25 °C		-	-	-100	nA
		V_{CB} = -60 V; I_E = 0 A; T_j = 150 °C		-	-	-50	µA
I_{CES}	collector-emitter cut-off current	V_{CE} = -60 V; V_{BE} = 0 V; T_{amb} = 25 °C		-	-	-100	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	-100	nA
h_{FE}	DC current gain	V_{CE} = -5 V; I_C = -1 mA; T_{amb} = 25 °C		200	350	-	
		V_{CE} = -5 V; I_C = -500 mA; T_{amb} = 25 °C	[1]	150	230	-	
		V_{CE} = -5 V; I_C = -1000 mA; T_{amb} = 25 °C	[1]	100	160	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -100 mA; I_B = -1 mA; T_{amb} = 25 °C		-	-110	-175	mV
		I_C = -500 mA; I_B = -50 mA; T_{amb} = 25 °C	[1]	-	-135	-180	mV
		I_C = -1000 mA; I_B = -100 mA; T_{amb} = 25 °C	[1]	-	-255	-340	mV
R_{CEsat}	collector-emitter saturation resistance		[1]	-	255	340	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = -1000 mA; I_B = -50 mA; T_{amb} = 25 °C	[1]	-	-0.95	-1.1	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = -5 V; I_C = -1000 mA; T_{amb} = 25 °C	[1]	-	-0.82	-0.9	V
t_d	delay time	I_C = -0.5 A; I_{Bon} = -25 mA; I_{Boff} = 25 mA; T_{amb} = 25 °C		-	11	-	ns
t_r	rise time			-	30	-	ns
t_{on}	turn-on time			-	41	-	ns
t_s	storage time			-	205	-	ns
t_f	fall time			-	55	-	ns
t_{off}	turn-off time	I_C = -0.5 A; I_{Bon} = 25 mA; I_{Boff} = 25 A; T_{amb} = 25 °C		-	260	-	ns

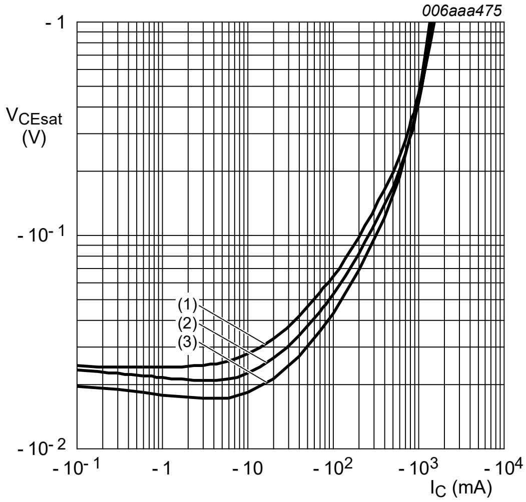
Symbol	**Parameter**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	9	15	pF
f_T	transition frequency	V_{CE} = -10 V; I_C = -50 mA; f = 100 MHz; T_{amb} = 25 °C		150	185	-	MHz
TR2; NPN resistor-equipped transistor							
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A; T_{amb} = 25 °C		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A; T_{amb} = 25 °C		-	-	1	µA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C		-	-	50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	900	µA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 20 mA; T_{amb} = 25 °C		30	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; T_{amb} = 25 °C	[1]	-	-	150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA; T_{amb} = 25 °C		-	1.1	0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 20 mA; T_{amb} = 25 °C		2.5	1.9	-	V
R1	bias resistor 1 (input)			3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.5	pF

[1] Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$



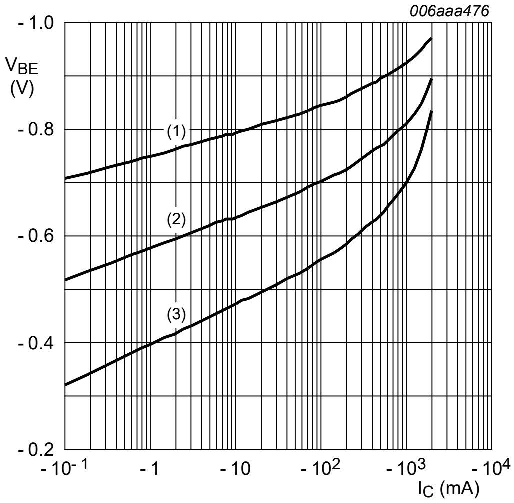
V_{CE} = -5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -55 °C

Fig. 5. TR1 (PNP): DC current gain as a function of collector current; typical values



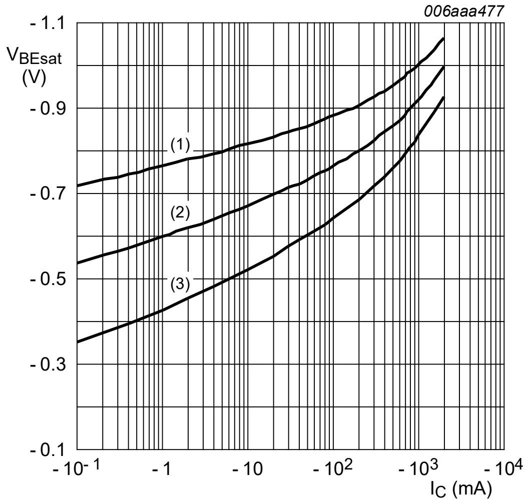
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -55 °C

Fig. 6. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



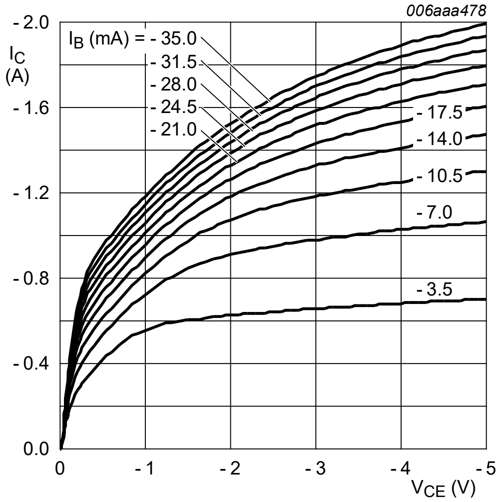
V_{CE} = −5 V
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values



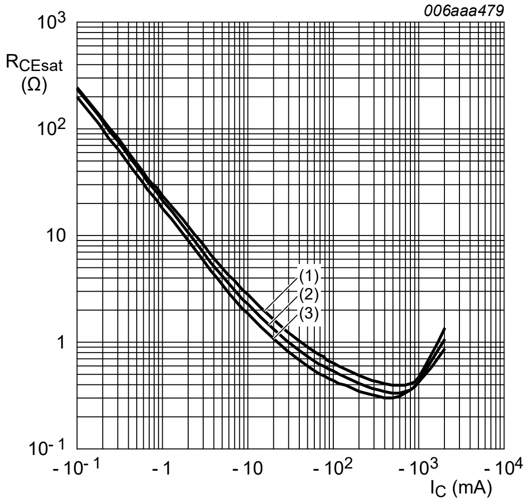
I_C/I_B = 20
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



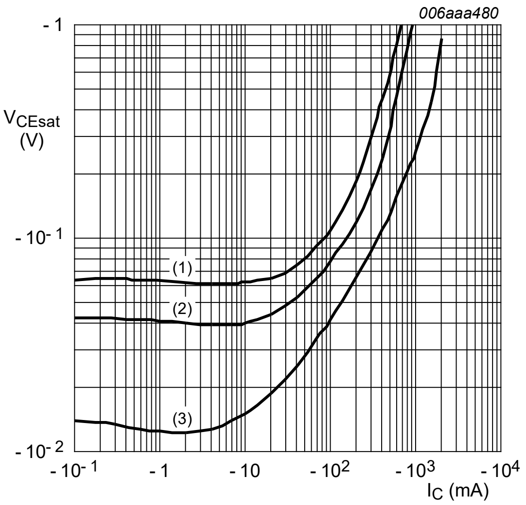
T_{amb} = 25 °C

Fig. 9. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values



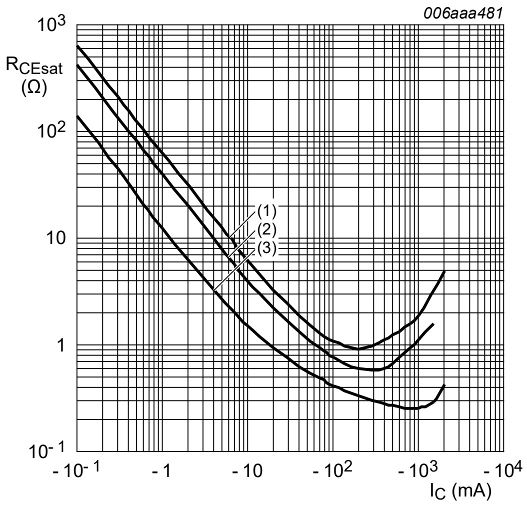
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -55 °C

Fig. 10. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



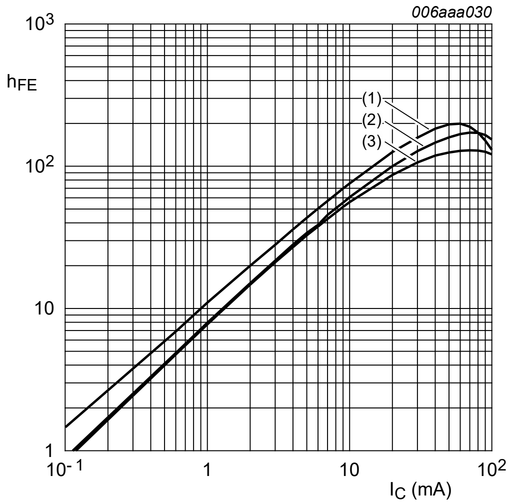
T_{amb} = 25 °C
(1) I_C/I_B = 100
(2) I_C/I_B = 50
(3) I_C/I_B = 10

Fig. 11. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



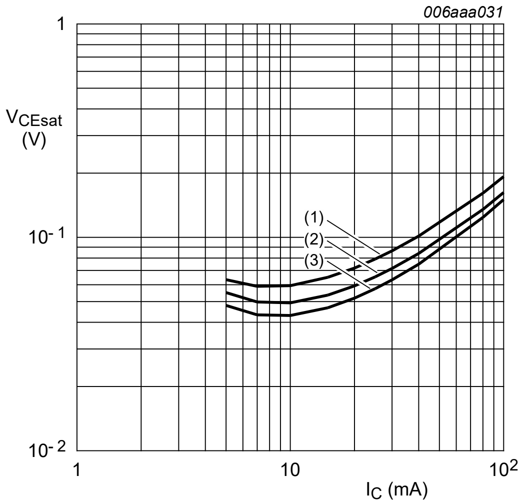
T_{amb} = 25 °C
(1) I_C/I_B = 100
(2) I_C/I_B = 50
(3) I_C/I_B = 10

Fig. 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



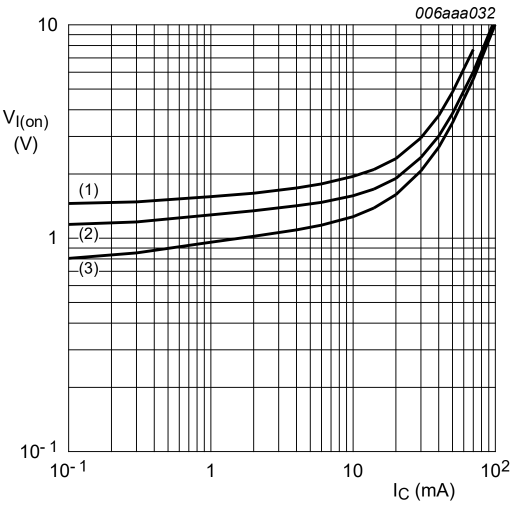
V_{CE} = 5 V
(1) T_{amb} = 150 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −40 °C

Fig. 13. TR2 (NPN): DC current gain as a function of collector current; typical values



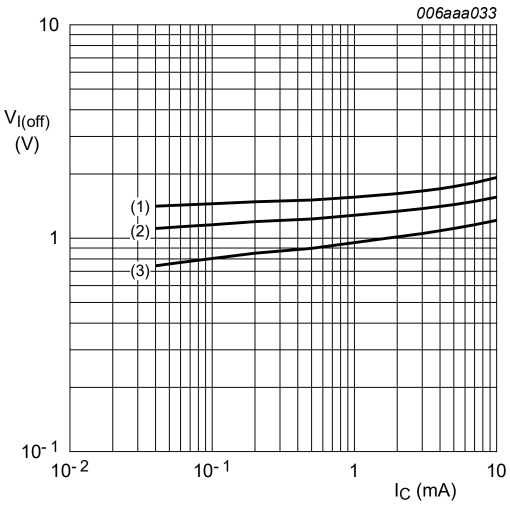
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 14. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 15. TR2 (NPN): On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 16. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

11. Test information

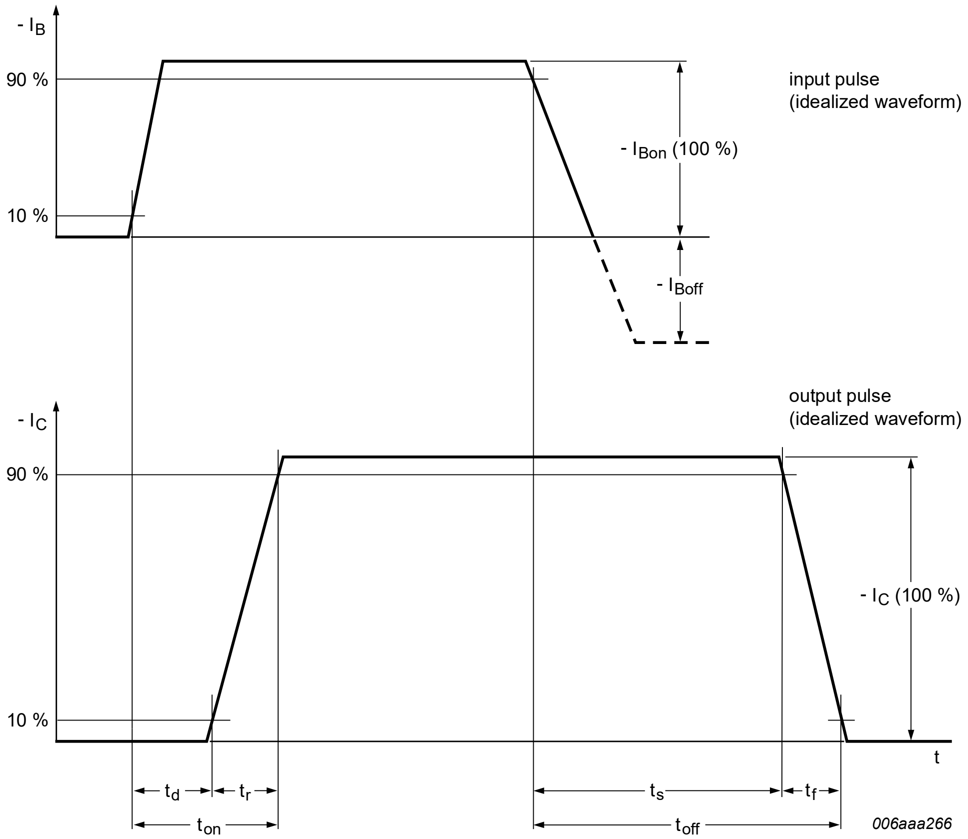
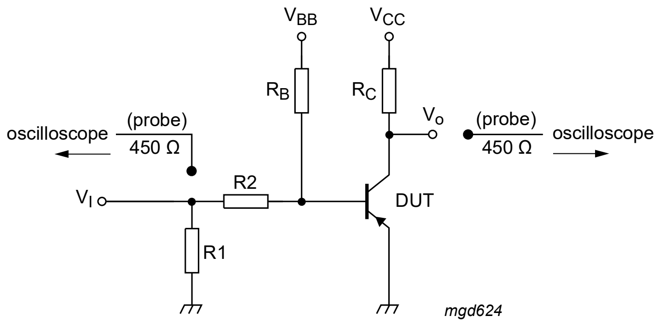


Fig. 17. Transistor switching time definition



I_I = -0.5 A; I_{Bon} = 25 mA; I_{Boff} = 25 mA; R1 = open; R2 = 100 Ω; R_B = 300 Ω; R_C = 20 Ω

Fig. 18. Test circuit for switching times

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

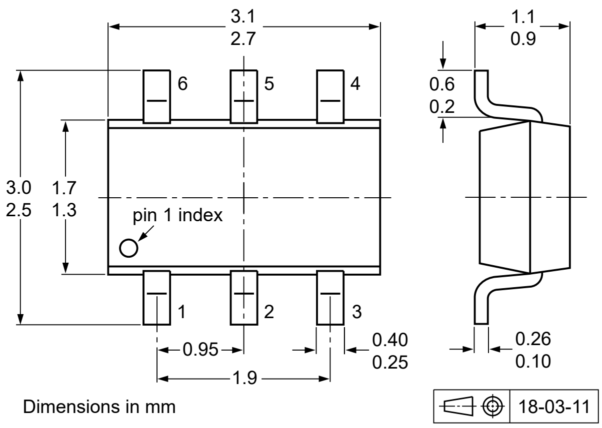


Fig. 19. Package outline TSOP6 (SOT457)

13. Soldering

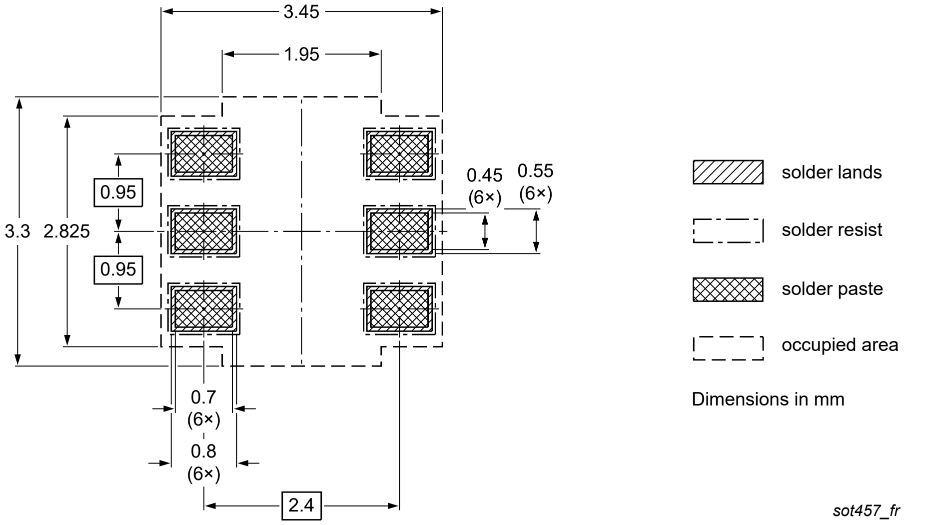


Fig. 20. Reflow soldering footprint for TSOP6 (SOT457)

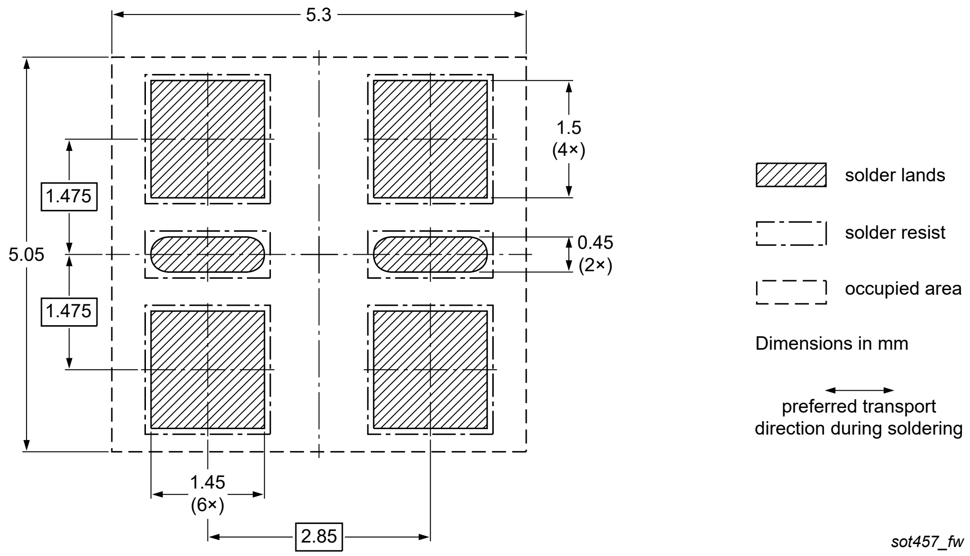


Fig. 21. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBLS6002D-Q v.1	20231026	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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